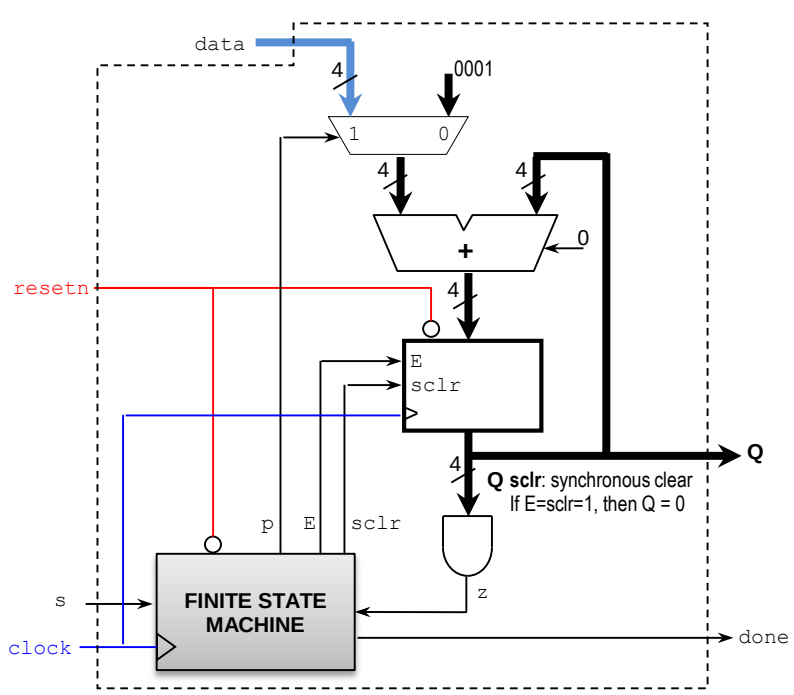
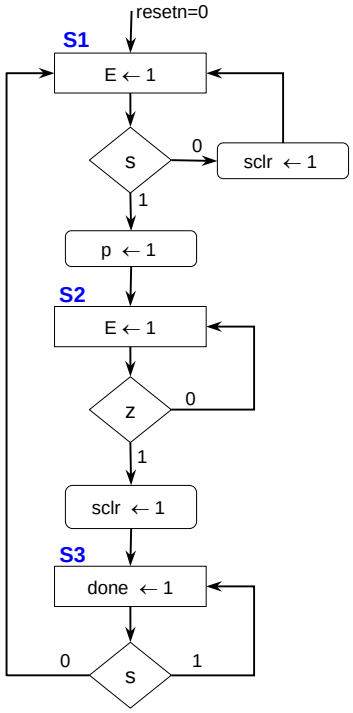
Homework 1

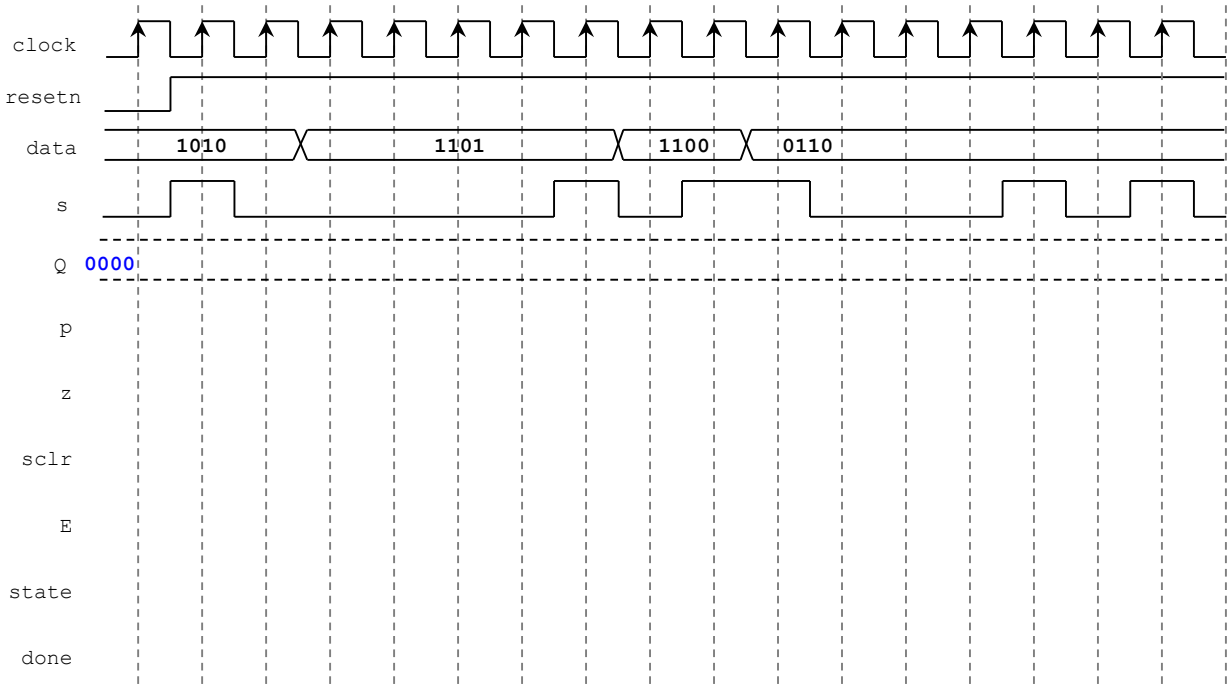
(Due date: January 18th @ 7:30 pm)
Presentation and clarity are very important! Show your procedure!

PROBLEM 1 (50 PTS)

- Given the following digital circuit that includes an FSM (in ASM form) and a datapath circuit:
  Note: Register. If E=1, sclr=0 → Parallel Load. If E=sclr=1 → Synchronous clear.
  - ✓ Complete the timing diagram of the digital circuit.
  - ✓ Write a structural VHDL code. You MUST create a file for i) 4-bit register, ii) 4-bit adder, iii) 4-bit Bus MUX 2-to-1, iv) Finite State Machine, and vi) Top file (where you will interconnect all the components). Provide a printout.
  - ✓ Write a testbench according to the timing diagram shown below. Simulate the circuit (Behavioral simulation). Verify that the simulation is correct by comparing it with the timing diagram you completed manually. Provide a testbench printout.







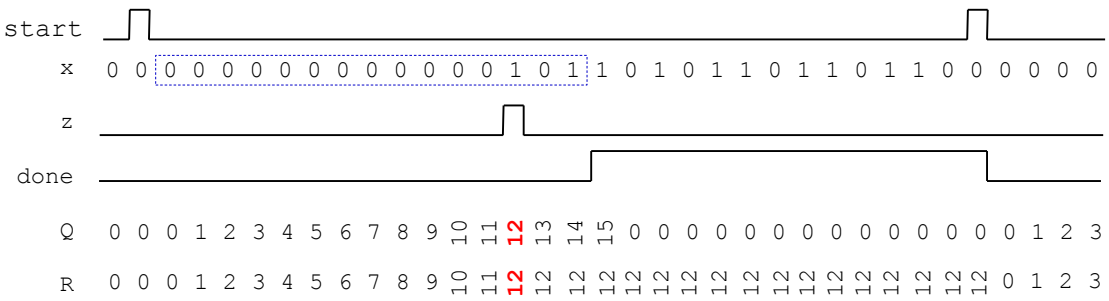
PROBLEM 2 (30 PTS)

- Design a serial leading-1 detector (datapath + FSM): A binary number of 15 bits is presented to the serial leading-1 detector, most significant bit first, on input X. The circuit generates the number of 0's that exist before the first 1. For example: If the number is 000000000000101, then the output should be 12. If the number is 000000000000000, then the output should be 15.

- Circuit inputs: X (serial data), start. Outputs: z (leading 1 detected), done (15 bits processed), and R (number of 0's before the first 1.
- The process begins with the assertion of the *start* signal (a clock pulse). For every bit, we increase a count Q (0 to 15). As long as the bits applied to X are 0, the output Z = 0, and we also increase a count R (0 to 15). When the first 1 is applied to X, then Z = 1 and we freeze the count R. For all bit values applied to X after the first 1 is applied, Z = 0. When the sequence is completed, we issue done='1'. To process another sequence, the input *start* becomes 1 for a clock cycle (here, done becomes 0). The counter R keeps the result until the *start* input is becomes 1 again.

  ✓ Sketch the circuit: FSM + Datapath. Specify all the I/Os of the FSM, as well as the signals connecting the FSM and the Datapath.
  Suggestion: The Datapath only needs two counters modulo-16 (Q and R). You can use the standard counter with *enable* and *sclr* inputs.

  ✓ Provide the State Diagram (in ASM form) of the FSM.



PROBLEM 3 (20 PTS)

- Calculate the result of the following operations, where the operands are signed integers. For the division, calculate both the quotient and the residue. **No procedure ≡ zero points.**

011001 × 11001	11001 × 1001	101001 ÷ 10001	0110101 ÷ 10101	10100 ÷ 0111